

1 Introduction

The EPS gate array is intended to integrate the three PLA's in the EPS digital section with five TTL packages. The result is reduced cost through a reduction in parts cost as well as a reduction in board space requirements for this logic.

The parts replaced are as follows: (as they appear on the EPS Digital Section Rev 3 schematic)

U29	82S153	\$2.50	BCU PLA
U30	74LS74	\$0.16	
U31	82S153	\$2.50	MMU PLA
U32	74LS138	\$0.16	
U33	82S153	\$2.50	ICU PLA
U34	74LS74	\$0.16	
U37	74LS161A	\$0.18	
U39	74LS74	\$0.16	
Y1		~\$1.20	Replace oscillator module with crystal
Y2		~\$1.20	Replace oscillator module with crystal

\$10.72 TOTAL

The latest quote for the gate array cost follows:

5000 pcs	\$4.01/ea.
10000 pcs	\$3.19/ea.
25000 pcs	\$3.03/ea.

This cost is based on a 1400 gate array in either a 64 pin skinny DIP or a 68 pin PLCC. The 1400 gate array is required from the stand-point of available I/O's, not from gate count requirements. Actually the logic requires approximately 100 gates to implement.

The decision on which package to put the array in is influenced by the following factors.

1. The 64 pin package does not have sufficient pins to support the 74LS138, therefore an external part must be used.
2. The 68 pin package would required a socket for mounting to the board, unless surface mounting were used.

The chip is designed independent of the package decision, and it is possible to change packages at a later time without incurring NRE charges.

2 Function

The gate array incorporates three main functions contained in the three PLA's. These functions are: Interrupt control, Memory management, and Bus control.

2.1 Interrupt control

The interrupt control functions accepts interrupt requests from the DMAC, DUART, and DOC. It prioritizes the interrupts as:

DOC = LEVEL 1
DMAC = LEVEL 2
DUART = LEVEL 3

and drives IPL1, and IPL0 to the CPU as follows:

/DUIRQ	/DMIRQ	/DOCIR	<i>Ipl</i>	/IPL1	/IPL0
0	0	0	1	0	0 4 3
0	0	1	1	0	0 4 3
0	1	0	1	0	0 4 3
0	1	1	1	0	0 4 3
1	0	0	1	0	1 5 2
1	0	1	1	0	1 5 2
1	1	0	1	1	0 6 1
1	1	1	1	1	1 7 0

When the CPU runs an interrupt cycle the gate array recognizes the processor state via the function pins and decodes the level presented on A1 and A2 to either signal the DMAC or DUART of the interrupt acknowledge, or assert VPA to the processor when a level 1 interrupt is being acknowledged.

2.2 Memory Management

The memory management function decodes the address space of the CPU and generates chip selects according to the following map.

	A23	A22	A21	A20	A19	A18	
	0	0	0	X	X	X	/OSRAM (user mode)
	0	0	0	X	X	X	/OSROM (supervisor mode)
	0	0	1	0	0	0	/DOC
	0	0	1	0	0	1	/DMAC
	0	0	1	0	1	0	/DUART
	0	0	1	0	1	1	/FDC
	0	0	1	1	0	0	/EXCS0 (external chip 0)
	0	0	1	1	0	1	/EXCS1 (external chip 1)
	0	0	1	1	1	0	/EXCS2 (external chip 2)
	0	0	1	1	1	1	UNUSED
8 Mbytes	0	1	X	X	X	X	/SRAM
4 Mbytes	1	0	X	X	X	X	UNUSED
8 Mbytes	1	1	0	X	X	X	/OSROM
	1	1	1	X	X	X	/OSRAM

2.3 Bus Control

The bus control function controls upper and low byte related signals for data transactions.

3 Pin Description

3.1 Inputs

- N* /AS - Address Strobe, low active. /AS comes from the 68000 and goes low to validate address and function code.
- N* /UDS,/LDS - Upper and Lower Data Strobes, low active. Come from the 68000 and used to control upper and lower bytes of memory.
- N* RW - Read , Write when low. Comes from the 68000, denotes direction of data transfer. Used to control OE and WE signals to memory.
- N* A2,A1 - Address bits 1 and 2. Contain interrupt level during interrupt acknowledge cycle. Decoded to generate /DUIAK, /DMIAC, and /VPA.
- N* A23, A22, A21, A20, A19, A18 - Address bits from CPU used to generate chip selects as shown previously in memory management section.
- N* FC2, FC1, FC0 - Function Code from CPU. Used to decode processor state as follows.
- | FC2 | FC1 | FC0 | |
|-----|-----|-----|-------------------------|
| 0 | 0 | X | USER MODE |
| 1 | 1 | 0 | SUPERVISOR MODE (RESET) |
| 1 | 1 | 1 | INTERRUPT ACKNOWLEDGE |
- PN* 10XI - Schmitt trigger input. Can be used as input from crystal to generate the 10MHz system clock on 10MO, or can be driven with externally generated 10MHz system clock in which case 10MO will be ignored. Used internally to generate 5M, 500K, and FCLK.
- PN* 8XI - Schmitt trigger input. Can be used as input from crystal to generate the 8MHz clock on 8M.
- N* /DUIRQ,/DMIRQ,/DOCIR - Low active interrupt requests from DUART, DMAC, and DOC respectively. Encoded into /IPL1, and /IPL0 to the CPU according to the table presented previously.
- PN* /OWN - Low active. Designates that DMAC is bus master when asserted. Used to control data flow on bus
- PN* /DBEN - Low active, Data Buffer Enable. Driven by DMAC to define data portion of cycle when it is bus master. Used to control data flow on bus.
- PN* /RAS - Low active, Row Address Strobe. Used to latch DA18 input during address phase of DRAM cycle.
- PN* /CAS - Low active, Column Address Strobe. Used to provide timing for driving /CAS0 and

/CAS1 outputs.

- DN* DA18 - Bit 18 of multiplexed address data bus from DOC. Used to generate CAS to the appropriate bank of ram.
- PN* /1M - low active, 1 Meg of sound ram. Used to generated /CAS0 and /CAS1 correctly based on the presence of an upper 512k of ram.
- DN* /DBUS - low active DOC Bus. Output from DOC which divides time on the sound ram bus between the DOC and the CPU. Used to select between DOC and CPU as a source for address and data on the sound ram bus.
- DN* AN1, CA2, CA1, CA0 - parallel inputs to internal 4 bit counter. When MUTE input is high the state of these pins is loaded into the counter 2 clocks after terminal count is reached.
- DN* MUTE - when high enables parallel loading of AN1, CA2, CA1, CA0 into internal counter on terminal. If low the counter will count modulo 16.
- DN* OE - High active. Enables output function of /FDC and /DOC. This pin must be tied low if the 64 pin package is used to allow /FDC and /DOC to function as inputs only since they will be generated by an external decoder. In the 68 pin version this signal is pulled high internal and is not bonded out.

3.2 Outputs

- DN* 10XO - Feedback output to 10MHz crystal.
- DN* 10MO - 10MHz output used to drive system clock when crystal is connected to 10XO and 10XI.
- DN* 8XO - Feedback output to 8MHz crystal.
- DN* 8M - 8MHz output when 8MHz crystal is connected to 8XI and 8XO.
- DN* 5M - divide by 2 of the 10MHz clock.
- DN* 500K - divide by 20 of the 10MHz clock.
- N* /IPL0, /IPL1 - Low active Interrupt lines to CPU. Asserted according to truth table presented in inputs section for /DMIRQ, /DUIRQ, /DOCIR.
- N* /DTACK - Data Transfer ACKnowledge, low active. Open collector output to CPU. CPU inserts waits states in bus cycle as long as this signal is not asserted. This chip asserts /DTACK on access to operating system ram and rom, and to the floppy disk controller.
- N* /VPA - Auto Vector, low active. This output instructs the CPU to generate it's own vector, when asserted during an interrupt acknowledge cycle. It is asserted by the gate array upon a level 1 interrupt acknowledge. Level 1 interrupts are generated by the DOC chip which does not output vectors during interrupt acknowledge.
- NOT MAY BE EXTERNAL*
- ALL AVEC*

- N* /OSRAM, - Low active, chip select to operating system ram. Assertion based on address map given in memory management section.
- N* /OSROM - Low active, chip select to operating system rom. Assertion based on address map given in memory management section.
- N* /SRAM - Low active. Input to DOC requesting CPU access to sound ram. Assertion based on address map given in memory management section.
- N* /FDC, /DOC, /DUART, /DMAC, /EXCS0, /EXCS1, /EXCS2 - Low active chip selects asserted based on address map given in memory management section. When /FDC and /DOC are pulldown together, an internal reset is generated to allow initialization of flip flops and counters for testing.
- may be external with 138*
 138EN - High active, enable to an external 74LS138 decoder. This output should be tied to the high active enable input of an external decoder when the 64 pin version of the gate array is used. Signal is not bonded out on 68 pin version.
- DN* /DMIACK - Low active, interrupt acknowledge to the DMAC.
- DN* /DUIACK - Low active, interrupt acknowledge to the DUART.
- DN* /UGWE, /LGWE - Low active write enables to sound ram, asserted on access to sound ram based on UDS, and LDS from the CPU. On DOC accesses of sound ram, both signals are asserted.
- N* /UWE, /LWE - Low active, upper and lower byte write enables to operating system ram.
- N* /URD, /LRD - Low active, upper and lower byte output enables to operating system ram and rom.
- DN* /CAS1, /CAS0 - Low active column address strobes used to select either internal or external banks of sound ram.
- EXTERNAL N* /244EN - Low active output enable to an external LS244 used to pull down data bus lines 0-3 during CPU reads of sound ram.
- ON* /U245E, /L245E - Low active output enables to two LS245's which connect upper and lower bytes of the CPU data bus with the sound ram data bus during CPU access of sound ram.
- DN* FCLK - Clock to analog section, generated by an internal 4 bit counter. FCLK toggles when the counter reaches terminal count.

4 Pad Assignments

Pad	Signal	I/O	Cell Name	Pad	Signal	I/O	Cell Name
1	A1	I	I2B	38	/OWN	I	I2B
2	FCLK	O	O2B	39	/DBEN	I	I2B
3	MUTE	I	I2B	40	/U245E	O	O2B
4	CA2	I	I2B	41	/UGWE	O	O2B
5	CA1	I	I2B	42	10MO	O	O2B
6	CA0	I	I2B	43	10XO	O	O2B
7	AN1	I	I2B	44	10XI	I	LIN, STIT
8	VDD	P		45	VSS	P	
9	/EXCS0	O	O2B	46	/DUART	O	O2B
10	/CAS1	O	O2B	47	NC		
11	/CAS1	O	O2B	48	A20	I	I2BP
12	OE	I	I2BP	49	138EN	O	O2B
13	/LRD	O	O2B	50	8XI	I	LIN, STIT
14	/EXCS1	O	O2B	51	8XO	O	O2B
15	/URD	O	O2B	52	8M	O	O2B
16	/RAS	I	I2B	53	5M	O	O2B
17	/OSROM	O	O2B	54	/LWE	O	O2B
18	/CAS	I	I2B	55	A23	I	I2B
19	/DBUS	I	I2B	56	A22	I	I2B
20	RW	I	I2B	57	A21	I	I2B
21	/EXCS2	O	O2B	58	/DUIAK	O	O2B
22	DA18	I	I2B	59	500K	O	O2B
23	/LDS	I	I2B	60	A2	I	I2B
24	/UDS	I	I2B	61	/DUIRQ	I	I2B
25	/AS	I	I2B	62	/DOCIR	I	I2B
26	/1M	I	I2B	63	A19	I	I2BP
27	/CAS0	O	O2B	64	/VPA	O	O2B
28	/CAS0	O	O2B	65	NC		
29	/DMAC	O	O2B	66	A18	I	I2BP
30	/244EN	O	O2B	67	/IPL0	O	O2B
31	/LGWE	O	O2B	68	/IPL1	O	O2B
32	/L245E	O	O2B	69	FC2	I	I2B
33	/DMIRQ	I	I2B	70	FC1	I	I2B
34	/DMIAK	O	O2B	71	FC0	I	I2B
35	/DTACK	O	ODN	72	/UWE	O	O2B
36	/FDC	I/O	H6T	73	/OSRAM	O	O2B
37	/DOC	I/O	H6T	74	/SRAM	O	O2B

5 Pinouts

5.1 64 Pin Shrink Dip

138EN	1	64	VSS
8XI	2	63	10XI
8X0	3	62	10XO
8M	4	61	10M
5M	5	60	/UGWE
/LWE	6	59	/U245E
A23	7	58	/DBEN
A22	8	57	/OWN
A21	9	56	/DOC
/DUIAK	10	55	/FDC
500K	11	54	/DTACK
A2	12	53	/DMIAK
/DUIRQ	13	52	/DMIRQ
/DOCIR	14	51	/L245E
NC	15	50	/LGWE
/VPA	16	49	/244EN
/IPL0	17	48	/CAS0
/IPL1	18	47	/1M
FC2	19	46	/AS
FC1	20	45	/UDS
FC0	21	44	/LDS
/UWE	22	43	DA18
/OSRAM	23	42	NC
/SRAM	24	41	RW
A1	25	40	/DBUS
FCLK	26	39	/CAS
MUTE	27	38	/OSROM
CA2	28	37	/RAS
CA1	29	36	/URD
CA0	30	35	/LRD
AN1	31	34	OE
VDD	32	33	/CAS1

10/1/54

8

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

VSS = 0V

Parameter	Symbol	Limits	Units
Power Supply Voltage	VDD	VSS - 0.3 to 7.0	V
Input Voltage	VIN	VSS - 0.3 to VDD + 0.3	V
Output Voltage	VOUT	VSS - 0.3 to VDD + 0.3	V
Output Current	IOUT	± 10	mA
Power Dissipation	PD	100	mW
Power Supply Current	IDD	± 40	mA
Storage Temp	TSTG	-65 to 150	°C

6.2 Recommended Operating Conditions

VSS = 0V

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Input Voltage	VIN	VSS		VDD	V
Operating Temperature	TOPR	0		70	°C

6.3 DC Characteristics

VSS = 0V, TA = 0 - 70 °C

Parameter	Symbol	Min	Typ	Max	Conditions
Static Current	IDDS			10uA	VIN = VDD or VSS IOH = IOL = 0
Input Leakage Current	IL	-1uA		1uA	VDD = 5.25V VIH = VDD VIL = VSS
High Input Voltage (except 10XI and 8XI)	VIH	2.2V			VDD = 5.25V
Low Input Voltage (except 10XI and 8XI)	VIL			0.6V	VDD = 4.75V
Schmitt high trigger (10XI and 8XI)	VT			2.4V	VDD = 5.25V
Schmitt low trigger (10XI and 8XI)	VT	0.6V			VDD = 4.75
Pull up resistor (OE, A18, A19, A20)	RPL	100K		900K	VDD = 5V
High output level (except /CAS0, /CAS1) (/CAS0, /CAS1)	VOH	VDD - 0.4V			VDD = 4.75V IOH = -2mA IOH = -4mA
Low output level (except /CAS0, /CAS1) (/CAS0, /CAS1)	VOL			VSS + 0.4V	VDD = 4.75V IOL = 6mA IOL = 12mA
Off state leakage current (/FDC, /DOC)	IOZ	-1uA		1uA	VDD = 5.25V VOH = VDD VOL = VSS

7 Simulation Results of Key Paths

FROM	TO		MIN	TYP	MAX
/AS	/DUIAK, /DMIAB,/VPA	TPLH TPHL	7NS 10NS	11NS 15NS	21NS 29NS
/AS	/OSRAM, /OSROM, /SRAM	TPLH TPHL	8NS 10NS	12NS 15NS	23NS 29NS
/AS	/DTACK	TPLH TPHL	11NS 11NS	17NS 16NS	32NS 31NS
/CAS	/CAS0, /CAS1	TPLH TPHL	6NS 8NS	10NS 12NS	18NS 23NS
10XI	/DTACK	TPLH TPHL	19NS 18NS	30NS 27NS	56NS 52NS
/DBEN, /UDS, /LDS	/DOC, /FDC, /DMAC, /DUART, /EXCS0, /EXCS1, /EXCS2	TPLH TPHL	12NS 15NS	19NS 24NS	36NS 46NS
/UDS, /LDS	/URD, /LRD	TPLH TPHL	7NS 12NS	11NS 19NS	20NS 35NS
/UDS, /LDS	/UWE, /LWE	TPLH TPHL	7NS 9NS	10NS 14NS	19NS 25NS
/UDS, /LDS	/UGWE, /LGWE	TPLH TPHL	7NS 10NS	11NS 15NS	20NS 29NS
/UDS, /LDS	138EN	TPLH TPHL	10NS 10NS	16NS 16NS	31NS 30NS
/UDS, /LDS	/U245E, /L245E	TPLH TPHL	8NS 15NS	13NS 23NS	24NS 39NS
/DBUS, /DOC,	/U245E, /L245E	TPLH TPHL	8NS 9NS	12NS 14NS	25NS 26NS
/DBUS	/244EN	TPLH TPHL	7NS 9NS	12NS 15NS	22NS 27NS
10XI	FCLK	TPLH TPHL	23NS 24NS	36NS 37NS	70NS 71NS
10XI	5M	TPLH TPHL	13NS 13NS	20NS 20NS	39NS 37NS
10XI	500K	TPLH TPHL	28NS 28NS	43NS 44NS	82NS 84NS

10XI	10MO	TPLH TPHL	9NS 11NS	14NS 18NS	26NS 33NS	25 34
10XI	10XO	TPLH TPHL	9NS 8NS	13NS 13NS	25NS 24NS	25 24
8XI	8M	TPLH TPHL	8NS 10NS	12NS 16NS	23NS 31NS	24
8XI	8XO	TPLH TPHL	8NS 8NS	13NS 12NS	24NS 24NS	24
/DMIRQ, /DUIRQ, /DO- CIR	/IPL0, /IPL1	TPLH TPHL	6NS 8NS	10NS 12NS	19NS 24NS	22 23

8 PLA Equations of current 82S153's

CUPL Version 2.11b Serial# 5-00001-095
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CREATED Mon Aug 03 17:37:59 1987

LISTING FOR LOGIC DESCRIPTION FILE: ICU.pld.pld

```

1:Name      ICU;
2:Partno    XXXXX;
3>Date      7/31/87;
4:Revision  0;
5:Designer  BOB YANNES;
6:Company   ENSONIQ;
7:Assembly  XXXXX;
8:Location  XXXXX;
9:
10:$INCLUDE PALASM.OPR
11:$define ++: $
12:$define * &
13:$define + #
14:$define / !
15:$define ( /*
16:$define ) */
17:
18:
19:/*~~~~~*/
20:/*THIS IS THE INTERRUPT CONTROL UNIT FOR THE MIRAGE II. IT      */
21:/*ENCODES THE INTERRUPT LEVEL, GENERATES INTERRUPT ACKNOWLEDGE  */
22:/*FOR PARTS WITH VECTORS AND GENERATES VPA FOR AUTOVECTORS.     */
23:/*ALSO DECODES SUPERVISOR PROGRAM AND INTERRUPT ACKNOWLEDGE STATES */
24:/*FOR MMU AND PROVIDES AN OPEN-COLLECTOR OUTPUT FOR DTACK      */
25:/*~~~~~*/
26:/* Allowable Target Device Types:82S153                        */
27:/*~~~~~*/
28:
29:
30:/*% Inputs %*/
31:
32:Pin 1      = !AS      ;      /* MPU ADDRESS STROBE      */
33:Pin 2      = FC2      ;      /* MPU STATUS BIT          */
34:Pin 3      = FC1      ;      /* MPU STATUS BIT          */
35:Pin 4      = FC0      ;      /* MPU STATUS BIT          */
36:Pin 5      = !DUIRQ   ;      /* DUART INTERRUPT        */
37:Pin 6      = !DMIRQ   FDC;  /* DMA CHANNEL INTERRUPT   */
38:Pin 7      = !DOCIRQ  Doc;  /* DOC INTERRUPT          */
39:Pin 8      = NDT      - ;      /* DTACK IN                */
40:Pin 18     = A2       ;      /* MPU ADDRESS             */
41:Pin 17     = A1       ;      /* MPU ADDRESS             */
42:
43:
44:
45:
46:
47:
48:
49:/*% Outputs %*/
50:
51:Pin 9      = NDTACK   - ;      /* OPEN COLLECTOR DTACK OUTPUT */
52:Pin 11     = !IFL1    ;      /* ENCODED INTERRUPT PRIORITY */
53:Pin 12     = !IFLO    ;      /* ENCODED INTERRUPT PRIORITY */
54:Pin 13     = !DUIACK  - ;      /* DUART INTERRUPT ACKNOWLEDGE */

```

Handwritten notes:
 FDC; 9A
 Doc; EN
 ✓ I
 a I

Version 2.11b Serial# 5-00001-095
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TED Mon Aug 03 17:38:11 1987

ING FOR LOGIC DESCRIPTION FILE: ICU.pld.pld

```
Pin 14      = !DMIACK ;      /* DMA CHANNEL INTERRUPT ACK      */
Pin 15      = !VPA      ;Avee /* SIGNAL TO MPU FOR AUTOVECTOR */
Pin 16      = !SUPER    ;      /* DECODED SUPERVISOR PROG STATE */
Pin 19      = !IACK     ;      /* DECODED INTERRUPT ACK STATE   */
```

5 0

/*& Declarations and Intermediate Variable Definitions &*/

/*& Logic Equations &*/

```
!IPL1 = (!(!DUIRQ) # !(!DMIRQ)) ;
!IPL0 = (!(!DUIRQ) # !(!DOIRQ)) ; (!(!DOIRQ) * !DMIRQ) ;
!DUIACK = (!(!IAS) & FC2 & FC1 & FCO & A2 & A1) ;
!DMIACK = (!(!IAS) & FC2 & FC1 & FCO & A2 & !A1) ;
!VPA = (!(!IAS) & FC2 & FC1 & FCO & !A2 & A1) ;
!SUPER = !(FC2 & FC1 & !FC0) ;
!IACK = !(FC2 & FC1 & FCO) ;
NDTACK = !(!IACK) ;
NDTACK.DE = !(NDT) ;
```

c Fuse Checksum (51EA)
c Transmit Checksum (FB88)

Version 2.11b Serial# 5-00001-095
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ING FOR LOGIC DESCRIPTION FILE: MMU.pld.pld

Name MMU;
Partno XXXXX;
Date 7/31/87;
Revision 0;
Designer BOB YANNES;
Company ENSONIQ;
Assembly XXXXX;
Location XXXXX;

\$INCLUDE PALASM.OPR

\$define +: \$
\$define * &
\$define + #
\$define / !
\$define (/*
\$define) */

/* ~~~~~ */
/* THIS IS THE MEMORY MANAGEMENT UNIT FOR THE MIRAGE II. IT */
/* GENERATES SYSTEM CHIP SELECTS FOR THE LOCAL RAM, LOCAL ROM, */
/* SHARED MEMORY AND I/O DEVICES. IT ALSO GENERATES THE DTACK */
/* SIGNAL FOR THE MPU WHICH MUST BE OPEN-COLLECTOR BUFFERED. */
/* ~~~~~ */
/* Allowable Target Device Types:82S153 */
/* ~~~~~ */

/* & Inputs & */

Pin 1	= !SUPER	;	/* DECODED SUPERVISOR PROG STATE	*/
Pin 2	= !AS	;	/* MPU ADDRESS STROBE	*/
Pin 3	= A23	;	/* MPU ADDRESS	*/
Pin 4	= A22	;	/* MPU ADDRESS	*/
Pin 5	= A21	;	/* MPU ADDRESS	*/
Pin 6	= !CAS	- ;	/* CAS CLOCK FROM DOC	*/
Pin 7	= !1M	- ;	/* 1 MEG MEMORY EXPANDER SELECTOR	*/
Pin 8	= !DBUS	- ;	/* BUS ARBITRATION SIGNAL FROM DOC	*/
Pin 19	? = DA18L	;	/* LATCHED DOC ADDRESS	*/
Pin 18	= !FDCDLY	;	/* DTACK DELAY FOR FLOPPY DISK	*/
Pin 17	= !IACK	;	/* DECODED INTERRUPT ACK STATE	*/

/* & Outputs & */

Pin 9	= !OSRAM	;	/* LOCAL RAM CHIP SELECT	*/
Pin 11	= !SRAM	;	/* SHARED RAM REQUEST	*/
Pin 12	= !CASO	- ;	/* DYNAMIC RAM SELECT (INT 256K)	*/
Pin 13	= !CAS1	- ;	/* DYNAMIC RAM SELECT (EXP 256K-1M)	*/
Pin 14	= !OSROM	;	/* LOCAL ROM CHIP SELECT	*/
Pin 15	= !IO	;	/* I-O DEVICE AREA CHIP SELECT	*/
Pin 16	= !DT	;	/* DTACK FOR MPU	*/

/* & Declarations and Intermediate Variable Definitions & */

DUPL Version 2.11b Serial# 5-00001-095
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 CREATED Fri Jul 31 15:01:28 1987

LISTING FOR LOGIC DESCRIPTION FILE: MMU.pld.pld

```

55:
56:
57:
58:
59:
60:/* & Logic Equations & */
61:!OSRAM = !(!(!AS)&!A23&!A22&!A21&!SUPER#(!AS)&A23&A22&A21&!IACK);
62:!SRAM = !(!(!AS)&!A23&A22);
63:!IO = !(!(!AS)&!A23&!A22&A21);
64:!OSROM = !(!(!AS)&A23&A22&!A21#(!AS)&!A23&!A22&!A21&!(!SUPER));
65:!DT = !(!(!OSRAM)#(!OSROM)#(!FDCDLY));
66:!CAS0 = !(!(!CAS)&!DBUS&!A23&A22&!A21#(!AS)#(!CAS)&!(!DBUS)&!DA18L&!1M);
67:!CAS1 = !(!(!CAS)&!DBUS&!A23&A22&A21#(!AS)#(!CAS)&!(!DBUS)&!1M&DA18L#(!
CAS)&!(!DBUS)&!(!1M));
68:
69:
  
```

Jedec Fuse Checksum (6654)
 Jedec Transmit Checksum (3067)

Fc2	Fc1	Fc0
1	1	0
1	1	1

/Super prog

/IACK

CUPL Version 2.11b Serial# 5-00001-095
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LISTING FOR LOGIC DESCRIPTION FILE: BCU.pld.pld

```
1:Name      BCU;
2:Partno    XXXXX;
3:Date      7/31/87;
4:Revision  0;
5:Designer  BOB YANNES;
6:Company    ENSONIQ;
7:Assembly  XXXXX;
8:Location  XXXXX;
9:
10:$INCLUDE PALASM.OPR
11:$define +=: $
12:$define * &
13:$define + #
14:$define / !
15:$define ( /*
16:$define ) */
17:
18:
19:/* ~~~~~ */
20:/* THIS IS THE BUS CONTROL UNIT FOR THE MIRAGE II.  IT GENERATES */
21:/* THE READ AND WRITE CONTROL SIGNALS AND THE ENABLE SIGNALS FOR */
22:/* THE DATA BUS ISOLATION BUFFERS FOR THE SHARED MEMORY AREA.    */
23:/* IT ALSO GENERATES A VALID DATA STROBE.                        */
24:/* ~~~~~ */
25:/* Allowable Target Device Types:82S153 */
26:/* ~~~~~ */
27:
28:/* & Inputs & */
29:
30:Pin 1      = !UDS      ; /*MPU UPPER DATA STROBE */
31:Pin 2      = !LDS      ; /*MPU LOWER DATA STROBE */
32:Pin 3      = RW        ; /*MPU READ-WRITE SIGNAL  */
33:Pin 4      = !OWN      - ; /*DMAC CONTROL ASSERTION */
34:Pin 5      = !SRAM      ; /*SHARED RAM REQUEST FROM MMU */
35:Pin 6      = !DBUS     - ; /*BUS ARBITRATION SIGNAL FROM DOC */
36:Pin 7      = !DBEN     - ; /*DMAC DATA BUS ENABLE    */
37:Pin 8      = !DOC      ; /*DOC CHIP SELECT         */
38:
39:/* & Outputs & */
40:
41:Pin 9      = !URD      ; /*UPPER READ SIGNAL      */
42:Pin 11     = !LRD      ; /*LOWER READ SIGNAL      */
43:Pin 12     = !UWE      ; /*UPPER WRITE SIGNAL     */
44:Pin 13     = !LWE      ; /*LOWER WRITE SIGNAL     */
45:Pin 14     = !UGWE     - ; /*UPPER SHARED RAM WRITE SIGNAL */
46:Pin 15     = !U245EN   - ; /*UPPER SHARED MEM D-BUFFER ENABLE */
47:Pin 16     = !244EN    - ; /*ENABLE FOR LOW NYBBLE PULL-DOWN */
48:Pin 17     = !LGWE     - ; /*LOWER SHARED RAM WRITE SIGNAL */
49:Pin 18     ✓ = !DS      - ; /*VALID DATA STROBE     */
50:Pin 19     = !L245EN   - ; /*LOWER SHARED MEM D-BUFFER ENABLE */
51:
52:/* & Declarations and Intermediate Variable Definitions & */
53:
54:
```

23 I
16 0

5 I
56 40

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ING FOR LOGIC DESCRIPTION FILE: BCU.pld.pld

/* & Logic Equations & */

```
!DS=!(!DOWN&(!(!UDS)#(!(!LDS))#(!(!DOWN)&(!(!DBEN)&(!(!UDS)#(!(!LDS)))));
!UFD=!(!RW&(!(!UDS)&(!(!DS)));
!LFD=!(!RW&(!(!LDS)&(!(!DS)));
!UWE=!(!RW&(!(!UDS)));
!LWE=!(!RW&(!(!LDS)));
!UGWE=!(!RW&!DBUS&(!(!SRAM)&(!(!UDS)));
!LGWE=!(!RW&!DBUS&(!(!SRAM)&(!(!LDS)));
!U245EN=!(!(!SRAM)&!DBUS&(!(!UDS)&(!(!DS)#(!(!DOC)&!DBUS)));
!L245EN=!(!(!SRAM)&!DBUS&(!(!LDS)&(!(!DS)#(!(!DOC)&!DBUS)));
!244EN=!(!(!SRAM)&!DBUS&RW);
```

c Fuse Checksum (751A)
c Transmit Checksum (475C)